**Solution of CA Lab Project**

Resources for code::

(To follow the link press ctrl + and left button of mouse)

Lab 3: Design of Half Adder and Full Adder using VHDL

* [CSIT\_Labs/3rd\_Semester/Computer\_Architecture/VHDL\_labs/Full\_Adder.vhd at main · sthsuyash/CSIT\_Labs (github.com)](https://github.com/sthsuyash/CSIT_Labs/blob/main/3rd_Semester/Computer_Architecture/VHDL_labs/Full_Adder.vhd)
* [CSIT\_Labs/3rd\_Semester/Computer\_Architecture/VHDL\_labs/Half\_Adder.vhd at main · sthsuyash/CSIT\_Labs (github.com)](https://github.com/sthsuyash/CSIT_Labs/blob/main/3rd_Semester/Computer_Architecture/VHDL_labs/Half_Adder.vhd)

Lab 4: Design of Multiplexer and De multiplexer using VHDL.

* [CSIT\_Labs/3rd\_Semester/Computer\_Architecture/VHDL\_labs/MUX\_4\_to\_1.vhd at main · sthsuyash/CSIT\_Labs (github.com)](https://github.com/sthsuyash/CSIT_Labs/blob/main/3rd_Semester/Computer_Architecture/VHDL_labs/MUX_4_to_1.vhd)

Lab 5: Design 4-bit binary-to-gray and gray-to-binary code converters using VHDL.

* [CSIT\_Labs/3rd\_Semester/Computer\_Architecture/VHDL\_labs/Binary\_to\_Gray\_Code.vhd at main · sthsuyash/CSIT\_Labs (github.com)](https://github.com/sthsuyash/CSIT_Labs/blob/main/3rd_Semester/Computer_Architecture/VHDL_labs/Binary_to_Gray_Code.vhd)
* [CSIT\_Labs/3rd\_Semester/Computer\_Architecture/VHDL\_labs/Binary\_to\_XS\_3\_code.vhd at main · sthsuyash/CSIT\_Labs (github.com)](https://github.com/sthsuyash/CSIT_Labs/blob/main/3rd_Semester/Computer_Architecture/VHDL_labs/Binary_to_XS_3_code.vhd)\

Lab 6: Design 8-bit parity generator and checker circuits using VHDL.

* [CSIT\_Labs/3rd\_Semester/Computer\_Architecture/VHDL\_labs/Parity\_Generator.vhd at main · sthsuyash/CSIT\_Labs (github.com)](https://github.com/sthsuyash/CSIT_Labs/blob/main/3rd_Semester/Computer_Architecture/VHDL_labs/Parity_Generator.vhd)
* [CSIT\_Labs/3rd\_Semester/Computer\_Architecture/VHDL\_labs/Parity\_Checker.vhd at main · sthsuyash/CSIT\_Labs (github.com)](https://github.com/sthsuyash/CSIT_Labs/blob/main/3rd_Semester/Computer_Architecture/VHDL_labs/Parity_Checker.vhd)

Lab 7: Design Encoder and Decoder using VHDL

* [CSIT\_Labs/3rd\_Semester/Computer\_Architecture/VHDL\_labs/Encoder\_8\_to\_3.vhd at main · sthsuyash/CSIT\_Labs (github.com)](https://github.com/sthsuyash/CSIT_Labs/blob/main/3rd_Semester/Computer_Architecture/VHDL_labs/Encoder_8_to_3.vhd)
* Decoder Code:

//Decoder code of VHDL

library IEEE;

use IEEE.std\_logic\_1164.all;

entity DEcoder is

port(A:in std\_logic;

B:in std\_logic;

D0:out std\_logic;

D1:out std\_logic;

D2:out std\_logic;

D3:out std\_logic);

end DEcoder;

architecture DecoderLogic of Decoder is

begin

D0<=(NOT A) AND (NOT B);

D1<=(NOT A) AND B;

D2<=A AND (NOT B);

D3<=A AND B;

end DecoderLogic;

Lab 10: Design 4-bit ALU using VHDL.

|  |
| --- |
| library IEEE; |
| use IEEE.STD\_LOGIC\_1164.ALL; |

|  |
| --- |
| use IEEE.NUMERIC\_STD.ALL; |
|  |

|  |
| --- |
| entity alu is |
| Port ( inp\_a : in signed(3 downto 0); |

|  |
| --- |
| inp\_b : in signed(3 downto 0); |
| sel : in STD\_LOGIC\_VECTOR (2 downto 0); |

|  |
| --- |
| out\_alu : out signed(3 downto 0)); |
| end alu; |

|  |
| --- |
|  |
| architecture Behavioral of alu is |

|  |
| --- |
| begin |
| process(inp\_a, inp\_b, sel) |

|  |
| --- |
| begin |
| case sel is |

|  |
| --- |
| when "000" => |
| out\_alu<= inp\_a + inp\_b; --addition |

|  |
| --- |
| when "001" => |
| out\_alu<= inp\_a - inp\_b; --subtraction |

|  |
| --- |
| when "010" => |
| out\_alu<= inp\_a - 1; --sub 1 |

|  |
| --- |
| when "011" => |
| out\_alu<= inp\_a + 1; --add 1 |

|  |
| --- |
| when "100" => |
| out\_alu<= inp\_a and inp\_b; --AND gate |

|  |
| --- |
| when "101" => |
| out\_alu<= inp\_a or inp\_b; --OR gate |

|  |
| --- |
| when "110" => |
| out\_alu<= not inp\_a ; --NOT gate |

|  |
| --- |
| when "111" => |
| out\_alu<= inp\_a xor inp\_b; --XOR gate |

|  |
| --- |
| when others => |
| NULL; |

|  |
| --- |
| end case; |
|  |

|  |
| --- |
| end process; |
|  |

|  |
| --- |
| end Behavioral; |